Fabrication techniques for low loss silicon nitride waveguides

Michael J. Shaw*, Junpeng Guo, G. Allen Vawter, Scott Habermehl, and Charles T. Sullivan
Sandia National Laboratories, Albuquerque, NM, USA 87185-1080

ABSTRACT

Optical waveguide propagation loss due to sidewall roughness, material impurity and inhomogeneity has been the focus of many studies in fabricating planar lightwave circuits (PLC's)[1,2,3] In this work, experiments were carried out to identify the best fabrication process for reducing propagation loss in single mode waveguides comprised of silicon nitride core and silicon dioxide cladding material. Sidewall roughness measurements were taken during the fabrication of waveguide devices for various processing conditions. Several fabrication techniques were explored to reduce the sidewall roughness and absorption in the waveguides. Improvements in waveguide quality were established by direct measurement of waveguide propagation loss. The lowest linear waveguide loss measured in these buried channel waveguides was 0.1 dB/cm at a wavelength of 1550 nm. This low propagation loss along with the large refractive index contrast between silicon nitride and silicon dioxide enables high density integration of photonic devices and small PLC's for a variety of applications in photonic sensing and communications.

Keywords: Waveguide, silicon nitride, optical loss, sidewall roughness, PLC, Si_3N_4

1. INTRODUCTION

Planar lightwave circuits (PLC's) have gained increased attention for use in hybrid photonic integrated circuits (PIC's) created either monolithically or in hybrid integration strategies[4]. Many application opportunities exist for compact PLC components in the telecommunications industry such as wavelength-division-multiplexing (WDM) optical power splitters, wavelength insensitive couplers, arrayed-waveguide gratings (AWG's) and thermooptic switches[5]. Sensor applications have recently gained added focus for creating devices such as resonant micro optic gyros (RMOG's)[6,7], Ring resonator coupled Mach-Zender interferometers[8], and many other sensing architectures. Although integrated circuit (IC) technology is very mature, the monolithic fabrication of micro scale waveguides has only recently been receiving increased focus and development. Many of the same process elements used in IC fabrication can be leveraged in creating passive waveguide structures in a CMOS fabrication line. Several strategies for reducing the losses attributed to Si_3N_4 waveguide fabrication have been reported in the past[9] and due to growing interest in PLC technologies there is renewed thrust in monolithically reproducing waveguides with low signal attenuation and small radius-of-curvature bends. The refractive index contrast between silicon nitride and silicon dioxide is large (2.0 vs. 1.45), allowing silicon nitride/silicon dioxide planar waveguides to have a small mode size and therefore low radiation bending loss compared with doped glass waveguides. Small waveguide bends can help put more photonic devices on a single silicon wafer, as well as be used in the design of compact, rugged high-Q waveguide ring resonators. High-Q waveguide ring resonators have applications for photonic sensors and optical logic switches. Silicon nitride is an integral material used in the fabrication of integrated circuits on silicon substrates and requires a relatively thin cladding when compared to glass systems. Thicker films impact both throughput and wafer curvature, making wafer handling difficult and sometimes deep UV lithography unfeasible. In reproducing waveguide devices, a robust process technology is necessary which can produce repeatable low loss waveguides, and incorporate all necessary process conditions in a CMOS fabrication line.

Micromachining Technology for Micro-Optics and Nano-Optics III, edited by
Eric G. Johnson, Gregory P. Nordin, Thomas J. Suleski, Proceedings of SPIE Vol. 5720
(SPIE, Bellingham, WA, 2005) 0277-786X/05/$15 · doi: 10.1117/12.588828

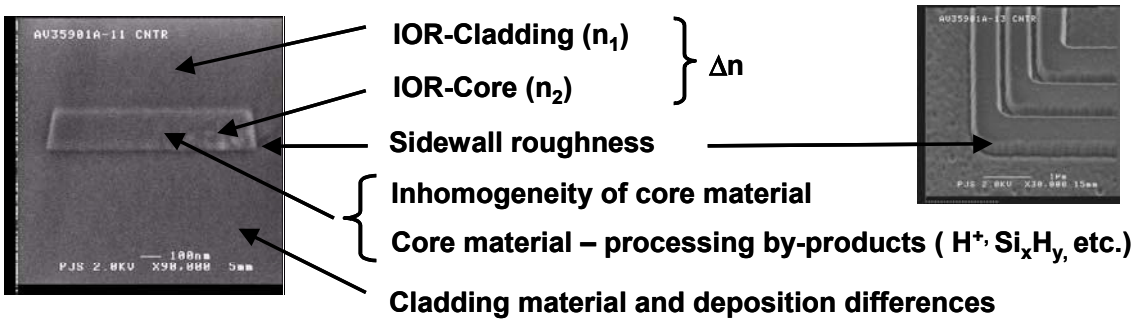

Figure 1. Major issues impacting loss mechanisms in the Si_3N_4/ SiO_2 waveguide material system.

Some major material and fabrication issues impacting linear losses are highlighted in Figure 1. Typically losses are attributed to two major sources. One is the scattering loss due to waveguide core/cladding interface roughness produced during processing. Another is the absorption loss due to H-O bonds in SiO_2 and H-N, Si-H in Si_3N_4. High-temperature annealing at 1050 -1200 °C can eliminate H-O bonds in SiO_2 and reduce H-N and Si-H bonds in Si_3N_4 leading to significant reductions in absorption loss[10].

In this paper the design of experiments (DOE's), fabrication processes, sidewall roughness smoothing strategies, measurement results, and the final loss results are detailed. Experiments were carried out to identify the best fabrication process for reducing propagation loss in silicon nitride/silicon dioxide single mode waveguides, while targeting a robust, reproducible waveguide fabrication technology. The first iteration of experiments, DOE1 & DOE2 produced 18 wafers with varying conditions, which were tested and evaluated for linear loss. A subsequent DOE3 experiment was manufactured which included the optimized set of processing conditions from the first set of experiments.

2. FABRICATION

Characterization structures were fabricated in the Microelectronics Development Laboratory (MDL), Class 1 clean room facility at Sandia National Laboratories. The fabrication of silicon nitride waveguides starts with a six inch diameter polished <100> silicon wafer. A two micron silicon dioxide (SiO2) film was grown on top of the silicon wafer using a thermal steam oxidation process followed by an additional three micron PECVD (plasma enhanced chemical vapor deposition) TEOS (tetraethylorthosilicate) deposition on top of the steam grown oxide producing a total of 5 microns of lower cladding SiO_2 film. Some of the lower cladding oxides used in these experiments were composed entirely of PECVD TEOS or a combination of steam oxidized substrate followed by steam oxidized amorphous polysilicon. The waveguide core is a silicon nitride (Si_3N_4) film deposited on top of the silicon dioxide layer using a LPCVD process. The waveguide devices were patterned with a deep UV (245 nm) photolithography stepper. The waveguides were etched using reactive ion etching (RIE) process to define the waveguide core structure, and then various techniques were used to reduce sidewall roughness before a final 4.0-micron silicon dioxide was deposited by either PECVD TEOS or high-density plasma (HDP).

3. ROUGHNESS MEASUREMENT

Sidewall roughness measurements were taken during the fabrication of waveguide devices for various processing conditions and at several points in the process flow. Critical dimension (CD) and sidewall measurements were taken on an Applied Materials NanoSEM 3D CD-SEM tool. The algorithm used to quantify sidewall roughness performs a linear fit to the edge points of the SEM signal, shown graphically in Figure 2.

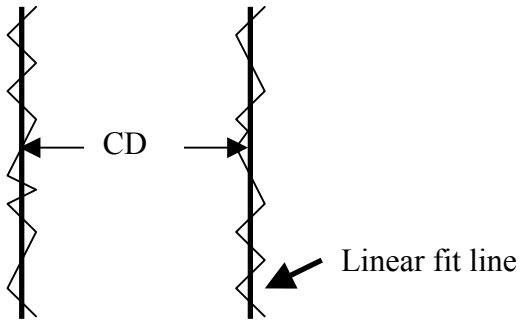

Figure 2. The roughness is the deviation between individual edge locations and a fitted line.

$$Roughness = 3 \bullet \sqrt{\sigma^2_{left-edge} + \sigma^2_{right-edge}} \qquad \textbf{[1]}$$

where σ (Sigma) is the standard deviation of the distances between individual edge locations and a fitted line. The critical dimensions (CD's) are reported as the measurement between the fitted lines. The NanoSEM 3D CD-SEM is capable of measuring a wide variety of roughness characteristics including top and bottom roughness and can discern between left and right side edges as well as identify discrete frequencies on sidewall features below 5 nm[11]. In this study the edge roughness result reported is calculated in a three-sigma fashion according to Equation [1].

4. LOSS MEASUREMENTS

Preparation of samples for waveguide loss measurements includes separation of the waveguide die, followed by 90 degree facet polishing on two sides, and then end-fire launching TE-polarized light from a 1550 nm wavelength tunable external-cavity laser In order to measure the curvature loss and linear loss, several PLC's as shown in Figure 3 were designed and fabricated. Figure 3 displays a shortened aspect ratio in order to better display the devices. In the bottom PLC of Figure 3, a lateral mode interference (LMI) type 3dB splitter evenly partitions the light into two output waveguides. The lower output waveguide is a straight waveguide. The upper output waveguide makes four 90° turns with a 500 micron radius of curvature before becoming a straight waveguide. Output power ratios of the upper and the lower waveguides were measured, which is recorded as R_1. Similarly, the middle circuit of Figure 3, has an upper straight waveguide and a lower waveguide with twelve 90° turns. The power transmission ratio of these waveguides is recorded as R_2. In the top circuit of Figure 3, light splits into a lower straight waveguide and an upper waveguide first making four 90° turns leading to a trombone section of 6mm length and an s-bend leading to the output of the circuit. The power transmission of these waveguides is recorded as R_3. All these turns are curved waveguides of 500 micron radius of curvature. The measured ratios of R_1, R_2, R_3 are then used to calculate the linear waveguide loss and bending loss for each experimental case.

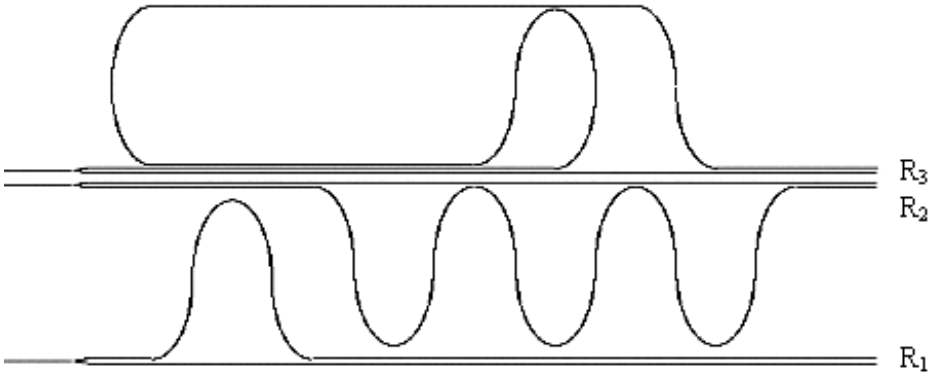

Figure 3 . PLC's for waveguide linear loss and curvature loss measurements.

5. EXPERIMENTAL

Various fabrication techniques were explored to reduce the sidewall roughness and absorption in the waveguide core as well as differing anneal temperatures, cycles and material deposition strategies. Several Design of Experiments (DOE's) were carried out using the Taguchi method with L_9 orthogonal arrays.[12] Experimental factors and their levels are shown in Table 1. One example of a L_9 experimental array is shown in Table 2.

Table 1. Factors and Levels

Factor	Levels		
	1	2	3
O – Oxide Type and deposition process	2 µm thermal oxide with 3 µm PETEOS lower cladding and 4 µm PETEOS upper cladding	5 µm PETEOS bottom cladding, 4 µm PETEOS upper cladding	2 µm thermal steam grown oxide with 3 µm thermal oxidized amorphous (poly)silicon 4 µm HDP oxide
A – Anneal frequency and location in flow	Anneal lower cladding for 3 hrs at 1100 °C, Anneal patterned Si_3N_4 core at 1100 °C for 3 hrs, Anneal after final cladding for 3 hrs. at 1100 °C	No lower cladding anneal, Anneal patterned Si_3N_4 core at 1100 °C for 3 hrs, Anneal after final cladding for 3 hrs. at 1100 °C	No lower cladding anneal, No patterned Si_3N_4 anneal Anneal after final cladding for 3 hrs. at 1100 °C
C – Chemical Mechanical Polishing (CMP) location in flow	CMP Lower cladding	CMP unpatterned Si_3N_4 surface only	CMP lower cladding and unpatterned Si_3N_4 surface
S - Smoothing strategy	Photo resist smoothing with RIE	Wet etch patterned Si_3N_4 in Hot Phosphoric acid solution	Steam oxidize RIE patterned Si_3N_4 at 1050 °C, and strip oxynitride in HF solution

Table 2. L_9 Orthogonal Matrix Experiment

Experiment (Wafer#)	O Oxide type and deposition process	A Anneals 1100 C	C CMP	S Smooth sidewalls
01	1	1	1	1
02	1	2	2	2
03	1	3	3	3
09	2	1	2	3
10	2	2	3	1
11	2	3	1	2
17	3	1	3	2
18	3	2	1	3
19	3	3	2	1

The Taguchi method relies on an additive model allowing the results of an orthogonal matrix of experiments to be averaged and large effects identified and characterized for interactions between variables. The method has a mathematical proof that is covered in reference 12. A "Smaller is better" approach was used with a quality characteristic "η_I" identified as the measured linear loss in decibels per centimeter, and then η_I was plotted showing the resulting major factor effects as the average of the equally represented factors of the orthogonal array. A simple example of how each effect was calculated is shown in equation [2].

$$m_{S3} = \frac{1}{3}\left(\eta_3 + \eta_9 + \eta_{18}\right) \qquad \textbf{[2]}$$

where m_{S3} is the linear loss measured for level 3 (steam oxidation) process. Experiments 3, 9, and 18 were all carried out with smoothing strategy 3 (steam oxidation), and the averaged effect of this smoothing strategy is given by (m_{S3} – m), where m is the overall mean of the DOE results.

Two 24-wafer lots were processed to support the first set of DOE experiments and die were measured for linear loss from 18 final wafers. Three sidewall roughness reducing strategies were employed in DOE1 and DOE2. Smoothing - 1, is a photoresist eroding strategy where an HBr-O2 chemistry is used in an Applied Materials DPS tool, with pressure modulation used to increase the erosion of photo resist sidewalls and smooth the photo resist prior to the silicon nitride etch step. The DPS tool is a low pressure, high-density, inductively coupled plasma etch tool. Smoothing – 2 is a wet etching strategy where a simple hot phosphoric acid bath at 180 °C, was used to etch some of the silicon nitride line away in an effort to smooth the sidewall. Smoothing – 3 was a high temperature steam oxidation strategy where the silicon nitride waveguide lines were oxidized at 1050 °C in an effort to oxidize asperities on the waveguide sidewall, followed by a Hydrofluoric acid (HF) wet process to strip the oxidized product, a process that had been previously shown to reduce roughness in a Si/SiO_2 system[13].

6. RESULTS

The smoothing results plotted in Figure 4 show relatively small differences between the smoothing strategies, although Lot 1 clearly had better results than Lot 2. We observed that the photolithography step quality had a larger influence on the sidewall roughness than any smoothing strategy employed.

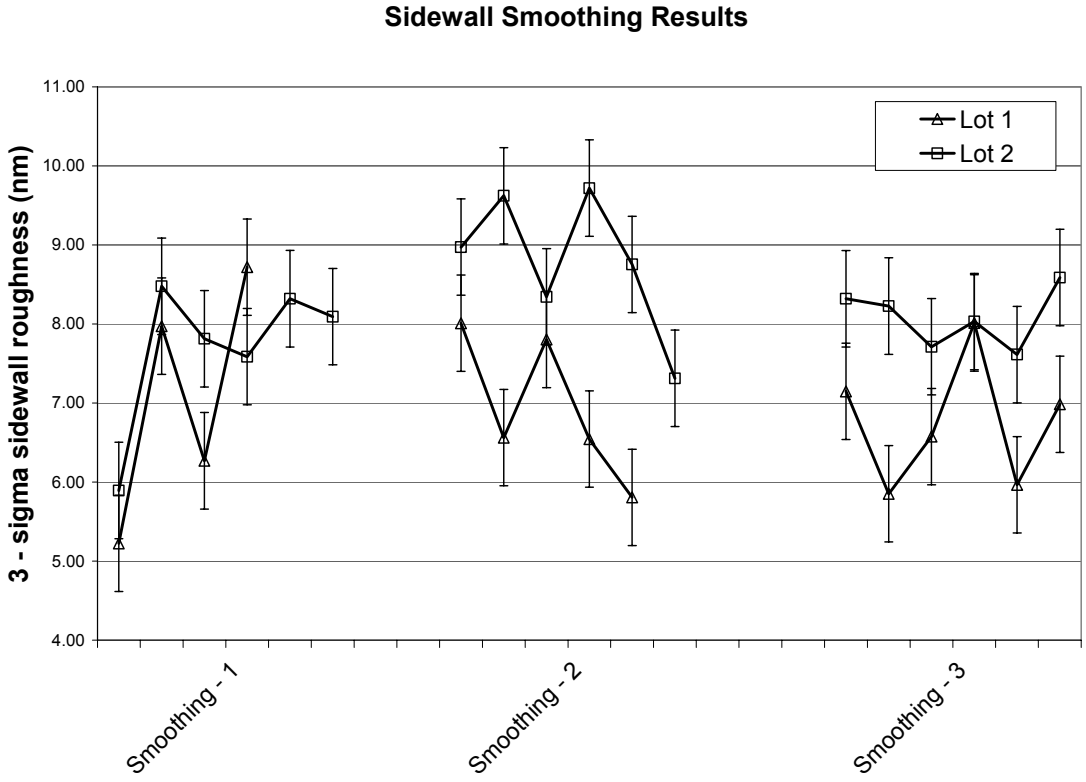

Figure 4. Roughness measurements for sidewall smoothing strategies 1, 2 & 3.

The error bars shown in Figure 4 are based on several measurements of the same waveguide lines on four different days at different times during the day, where the equipment was calibrated each day at the beginning of the first shift. The roughness numbers recorded in this experiment are small and in a range where slight variations may not be discernible from the day-to-day calibration variation. Measurements taken from a full set of wafers with differing processes can give an indication of how the process parameters have affected overall results, however, any attempt to investigate a before and after type experiment may be misleading due to the day-to-day variation in the 3D NanoSEM tool. Calibration of the CD-SEM prior to each roughness measurement may produce more consistent results and reduce the variation from day to day that is displayed as error bars in these examples.

Table 3 shows the best overall fabrication processes for reducing linear loss, based on DOE1 and DOE2 experiments and linear loss measurements for all levels that were investigated.

Table 3. Overall best processing results from DOE1 and DOE2 for reducing linear loss.

Process	Level	Best result
O – Oxide Type and deposition process	2	All PETEOS cladding
A – Anneal frequency and location in flow	1	Anneal lower cladding for 3 hrs at 1100 °C
AT – Patterned Si_3N_4 Anneal Time	2	Anneal patterned Si_3N_4 core at 1100 °C for 6 hrs.
C – Chemical Mechanical Polishing (CMP) location in flow	3	CMP lower cladding and unpatterned Si_3N_4 surface
S - Smoothing strategy	3	Steam oxidize RIE patterned Si_3N_4 at 1050 °C, and strip oxidized product in HF solution

Overall major effects shown in Figure 5 show that the sidewall smoothing strategy 3, steam oxidation with HF strip had the largest effect in reducing linear loss. However, smoothing plots shown in Figure 4 do not reflect that the steam oxidation is smoothing the sidewalls to a significant degree.

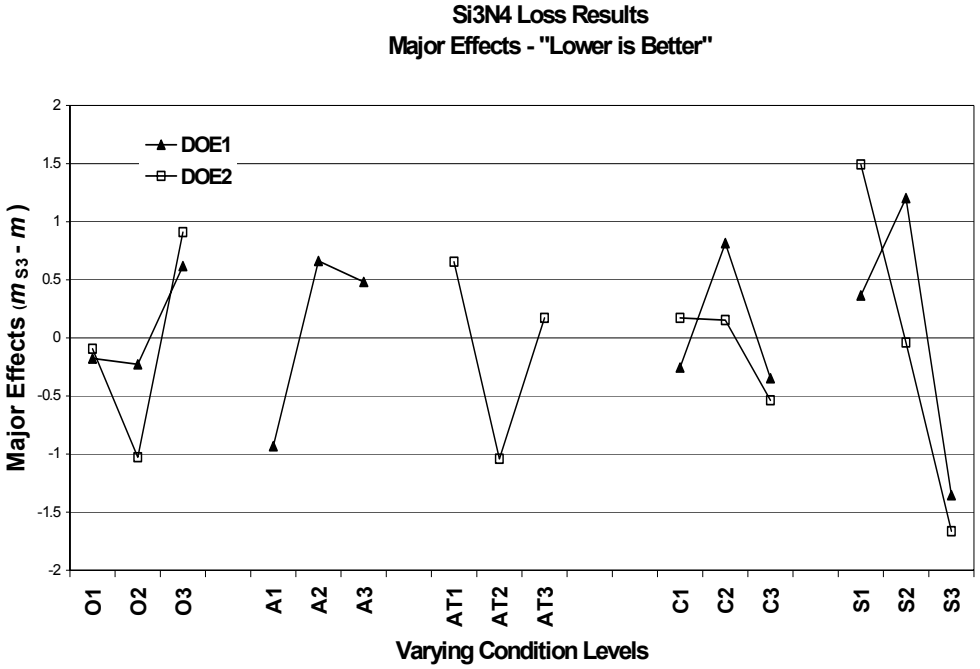

Figure 5. Waveguide loss results displayed as Major Effects calculated from Equation 2. DOE1 and DOE2 differ by the anneal experiment levels where An = anneal locations in the flow, and ATn = anneal duration time. Sidewall smoothing strategy 3, steam oxidation and HF strip show the biggest effect in reducing the linear loss.

FTIR scans shown in Figure 6 were performed on blanket Si_3N_4 films for the conditions: as deposited, annealed at 1200 °C, and annealed at 1200 °C with a subsequent steam oxidation at 1050 °C. The data displayed in the plot has been exaggerated so as to allow viewing of each individual curve. Curve data from wavenumber 1800 to 4000 have multiplied by 50. Curve (b) and (c) have had 0.4 and 0.8 added to the data respectively. Figure 6 curve (a) shows the N-H stretching vibration centered in the region 3350 (cm^{-1}) and the Si-H peak centered in the ~2250 (cm^{-1}) region[14]. It appears that the high temperature anneal at 1200 °C has eliminated the hydrogen peaks shown in curve (b) and that the subsequent steam oxidation at 1050 °C for 1 hr. has had little effect on the film shown in curve (c) with respect to hydrogen. The steam oxidation step does not appear to affect the hydrogen content of the Si_3N_4 waveguide material to a detectable degree, indicating that either significant sidewall smoothing has occurred or some other aspect of the material has changed due to the oxidation or stripping procedure.

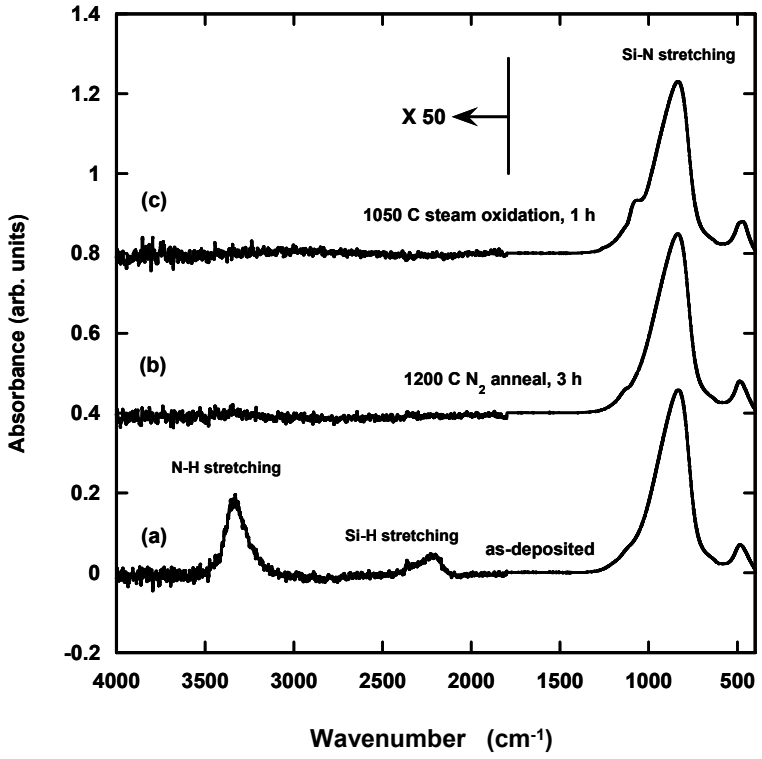

Figure 6, curves (a), (b) and (c). FTIR scan of Si_3N_4 blanket film as deposited, annealed at 1200 degrees for 3 hrs., and 3 hr. 1200 °C anneal - followed by steam anneal at 1050 degree C for 1 hr. (a) As deposited Si_3N_4 film showing N-H and Si-H stretching. (b) After 1200 °C anneal the peaks are vacant. (c) 3 hr. 1200 °C anneal followed by 1050 °C steam oxidation for 1 hr.

Based on measured results from the first set of experiments a second set of experiments were performed that used the ideal process parameters from the first two DOE's and further explored the strategies that had the largest impact on reducing loss. The results of the experiments ran on the third DOE can be seen in Table 4.

Table 4. Results from DOE3 with optimized processes and anneal experiments, all losses are for the TE mode.

Wafer #	Linear Loss (dB/cm)	Process
Wafer 6	1.45 dB/cm	1200 °C, final anneal, no steam, strip in HF
Wafer 10	0.16 dB/cm	1200 °C, no final anneal, 15 min. steam, strip in HF
Wafer 18	0.25 dB/cm	1200 °C, no final anneal, 30 min. steam, no strip in HF
Wafer 19	0.42dB/cm	9hrs. @1100 °C, no final anneal, 1 hr. steam, strip in HF
Wafer 22	**0.108 dB/cm**	**1200 °C, no final anneal, 1 hr. steam, strip in HF**
Wafer 23	0.75 dB/cm	1200 °C, final anneal, 1hr. steam, strip in HF

7. DISCUSSION

The lowest linear waveguide loss measured in these buried channel waveguide experiments was 0.1 dB/cm. This low propagation loss along with the large refractive index contrast between silicon nitride and silicon dioxide enables high-density integration of photonic devices and small PLC's for a variety of applications in photonic sensing and communications.

Several valuable process effects were identified through this broad experimental space while carrying out this research. The type of oxide deposited as the upper and lower cladding has the most significant influence on loss. In the case where high-density plasma oxide (HDP) was deposited over the patterned silicon nitride waveguide structures, the loss was so high as to prevent some loss measurements. The major-effect data for this oxide strategy was averaged based on the only measurable data point and then applied to the rest of the data based on a qualitative scale. The use of PETEOS deposited at low temperature was shown to be the best performing oxide cladding process. Furthermore, increased losses were observed in devices that had been annealed after the final cladding had been deposited, indicating there was a significant temperature induced change at the final cladding stage of the process. Some authors have suggested that a final anneal is necessary to remove OH bonds in the cladding oxide[10]. However, we have not found this to be the case in these experiments, where the losses for devices that received the final anneal were increased from the unannealed at 0.1 dB/cm range to as high as 0.75 db/cm for annealed with otherwise identical processing parameters. The loss due to final annealing may be caused by stress at the interface due to the effects of annealing and the coefficient of thermal expansion (CTE) mismatch between the Si_3N_4 and the oxide[15].

Roughness measurements taken for waveguides fabricated with the differing smoothing strategies were compared and it was found that other processing parameters were dominating the losses, suggesting that the predominant mechanism contributing to loss is scattering due to material inhomogeneity or core defects and H bonds in the Si_3N_4[13]. A large benefit was observed for the steam oxidation strategy with the oxidized material removed in a wet strip process. Monitor wafers were processed in the steam oxidation sequence with no pattern to investigate the material property changes during the anneal progression. FTIR scans show that hydrogen has been, for the most part, eliminated after the first 1200 °C anneal, and that the second steam oxidation anneal at 1050 °C has had little effect on the core material. The oxidation may have reduced the sidewall roughness to an extent that is not measurable in the CD-SEM.

8. CONCLUSION

Several design of experiments were executed with a specific strategy for reducing sidewall roughness and material inhomogenity in the silicon nitride/silicon dioxide material system. An optimized process was developed for Si_3N_4/SiO_2 waveguide manufacturing so as to produce very low loss waveguide devices in a fully operational CMOS fabrication line. It was discovered that the type of oxide deposition process over the patterned waveguide material had the most significant impact in controlling loss, an effect not found in literature or prior experiments. Finally, it was shown that a Taguchi type DOE approach to waveguide fabrication process development has lead to dramatic improvements in PLC loss while insuring the process technology has combined all necessary process steps in an innovative robust process technology.

Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94-AL85000.

[1] Elson, J. Merle, "Scattering losses from planar waveguides with material inhomogeneity", Waves Random Media ; April 2003; v.13, no.2, p.95-105.
[2] Elson, J. Merle, "Theoretical comparison of scattering losses in planar waveguides with wall roughness and core inhomogeneity", Proceedings of SPIE - The International Society for Optical Engineering ; 2002; v.4780, p.32-39.
[3] Bulla, Douglas Anderson Pereira; Borges, Ben-Hur Viana; Romero, Murilo Araujo; Morimoto, Nilton Itiro; Goncalves Neto, Luiz, "Design and fabrication of SiO{sub 2}/Si{sub 3}N{sub 4} integrated-optics waveguides on silicon substrates", IEEE Transactions on Microwave Theory and Techniques ; January 2002; v.50, no.1, p.9-12
[4] K. Kato, Y. Tohmori, Quantum Electronics, Vol. 6, No. 1, Jan./Feb. 2000.
[5] A. Himeno, K. Kato Quantum Electronics, Vol. 4, No. 6, November/December 1998, p913.
[6] K. Suzuki, K. Takiguchi, J. of Lightwve Tech., Vol. 18, No1, January 2000, p 66-72.
[7] C. Ford, R. Ramberg, K. Johnson, IEE AES system magazine, December 2000, p 33-36.
[8] J. Guo, G. A .Vawter, M. Shaw, G. Hadley, P Esherick, A. Jain, C. Alford, C. Sullivan, Characterization of Si3N4/SiO2 planar lightwave circuits and ring resonators, Proceedings of SPIE - The International Society for Optical Engineering ; 2004; v.5350, p.13-22
[9] Stutius, W.; Streifer, W., "Silicon Nitride Films On Silicon For Optical Waveguides." Applied Optics ; Dec 1977; v.16, no.12, p.3218-3222
[10] C. H. Henry, R. F. Kazarinov, H. J. Lee, K. J. Orlowsky, and L. E. Katz, "Low loss Si3N4 -S102 optical waveguides on Si", *Applied Optics,* 1 July 1987 / Vol. 26, No. 13 / p2621
[11] Marschner, Thomas; Lee, Anice; Fuchs, Stefan; Volkel, Lars; Stief, Christian, 193nm resist roughness characterisation and process propagation investigation using a CD-SEM", Proceedings of SPIE - The International Society for Optical Engineering ; 2004; v.5375, no.PART 1, p.477-485.
[12] Phadke, M., Quality Engineering Using Robust Design, Prentice Hall 1989.
[13] Kevin K. Lee, Desmond R. Lim, and Lionel C. Kimerling, Fabrication of ultralow-loss Si/SiO2 waveguides by roughness reduction, Optics Letters, Vol. 26, No. 23/ December1, 2001, p1888.
[14] Ay, F.; Aydinli, A., "Comparative investigation of hydrogen bonding in silicon based PECVD grown dielectrics for optical waveguides", Optical Materials; June 2004; v.26, no.1, p.33-46
[15] S. Janz, P. Cheben, H. Dayan, and R. Deakos, "Measurement of birefringence in thin-film waveguides by Rayleigh scattering", Optics Letters , Vol. 28, No. 19, p. 1778